Attorney Docket: RPS920010127US1/2280P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Date: August 8, 2008

Robert T. BAILIS et al. Confirmation No: 5286

Serial No: 10/016,449 Group Art Unit: 2117

Filed: December 10, 2001 Examiner: John J. Tabone, Jr.

Title: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A

DEBUGGER CLIENT WITHIN THE ASIC

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AMENDMENT

Please amend the application as indicated on the following pages:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page **5** of this paper.